P2371/37178.830083.000 for AN APPARATUS FOR HANDLING REGISTER WINDOWS IN AN OUT-OF-ORDER PROCESSOR filed concurrently herewith by Ramesh Panwar and Dani Y. Dakhil; Ser. No. 08/881,847 identified as Docket No. P2372/37178.830084.000 for AN APPARATUS FOR DELIVERING PRECISE TRAPS AND INTERRUPTS IN AN OUT-OF-ORDER PROCESSOR filed concurrently herewith by Ramesh Panwar; Ser. No. 08/881,728 identified as Docket No. P2398/37178.830085.000 for NON-BLOCKING HIERARCHICAL CACHE THROTTLE filed concurrently herewith by Ricky C. Hetherington and Thomas M. Wicki; Ser. No. 08/881,727 identified as Docket No. P2406/37178.830086.000 for NON-THRASHABLE NON-BLOCKING HIERARCHICAL CACHE filed concurrently herewith by Ricky C. Hetherington, Sharad Mehrotra and Ramesh Panwar; Ser. No. 08/881,065 identified as Docket No. P2408/37178.830087.000 for INLINE BANK CONFLICT DETECTION AND RESOLUTION IN A MULTI-PORTED NON-BLOCKING CACHE filed concurrently herewith by Ricky C. Hetherington, Sharad Mehrotra and Ramesh Panwar; and Ser. No. 08/882,613 identified as Docket No. P2434/37178.830088.000 for SYSTEM FOR THERMAL OVERLOAD DETECTION AND PREVENTION FOR AN INTEGRATED CIRCUIT PROCESSOR filed concurrently herewith by Ricky C. Hetherington and Ramesh Panwar, the disclosures of which applications are herein incorporated by this reference.

INT-CL: [6] G06F 9/00
US-CL-ISSUED: 712/216; 712/23, 712/24, 712/25, 712/205, 712/214, 712/215, 712/231, 712/233
US-CL-CURRENT: 712/216; 712/205, 712/214, 712/215, 712/23, 712/231, 712/233, 712/24, 712/25
FIELD-OF-SEARCH: 395/800.23, 395/800.24, 395/800.25, 395/390, 395/392, 395/580, 395/501, 395/582, 712/23, 712/24, 712/75, 712/205, 712/214, 712/215, 712/231, 712/216, 712/233

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4970641	November 1990	Hester et al.	361/200
☐	5333280	July 1994	Ishikawa et al.	395/375
☐	5367650	November 1994	Sharangpani et al.	395/800.23
☐	5442757	August 1995	McFarland et al.	395/800.23
☐	5560032	September 1996	Nguyen et al.	395/800.23
☐	5603047	February 1997	Caulk et al.	395/800.23
☐	5655096	August 1997	Branigin	395/376

OTHER PUBLICATIONS

Smith, Alan Jay; "Cache Memories," Computing Surveys, vol. 14, No. 3, Sep. 1982, pp. 473-530.

ART-UNIT: 273
PRIMARY-EXAMINER: An; Meng-Ai T.
ASSISTANT-EXAMINER: Nguyen; Dzung C.
ATTY-AGENT-FIRM: Langley; Stuart T. Sirr; Francis A. Holland & Hart LLP

ABSTRACT:

A processor that executes coded instructions using an instruction scheduling unit receiving the coded instructions and issuing an instruction for execution. A replay signaling device generates a signal indicating when the instruction failed to execute properly within a predetermined time. A replay device within the instruction scheduling unit responsive to the signaling device then reissues the instruction for execution.

18 Claims, 7 Drawing figures

WEST

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L4: Entry 8 of 53 File: USPT Aug 24, 1999

US-PAT-NO: 5941984
DOCUMENT-IDENTIFIER: US 5941984 A

TITLE: Data processing device

DATE-ISSUED: August 24, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mohri; Atsushi	Tokyo	N/A	N/A	JPX
Yamada; Akira	Tokyo	N/A	N/A	JPX
Yoshida; Toyohiko	Tokyo	N/A	N/A	JPX

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	Tokyo	N/A	N/A	JPX	03

APPL-NO: 8/ 857461
DATE FILED: May 16, 1997

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	9-019401	January 31, 1997

INT-CL: [6] G06F 15/16
US-CL-ISSUED: 712/218; 712/23, 712/24
US-CL-CURRENT: 712/218; 712/23, 712/24
FIELD-OF-SEARCH: 395/800.23, 395/800.24, 395/394, 712/218, 712/23, 712/24

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5636353	June 1997	Ikenaga et al.	395/394
☐	5805852	September 1998	Nakahashi	395/394

OTHER PUBLICATIONS

"The MMA: A Long-instruction-Word Multimedia processor"; Microprocessor Forum, Oct. 22, 1996; Shumske Kamijo; pp. 1, 4, & 5.
"Phillips Hopes to Displace DSPs with VLIW"; Microprocessor Report, Dec. 5, 1994; Brian Case; pp. 12 to 15.

ART-UNIT: 273
PRIMARY-EXAMINER: Treat; William M.
ABSTRACT:

A VLIW microprocessor in which bypaths for transferring data among pipelines are

A VLIW microprocessor in which bypaths for transferring data among pipelines are incorporated between a plurality of execution units such as a memory access unit and an integer operation unit. The data on the bypaths is directly transferred to target units according to a control signal generated by a bypath processing control circuit.

13 Claims, 40 Drawing figures

WEST

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L4: Entry 9 of 53 File: USPT May 4, 1999

US-PAT-NO: 5901301
DOCUMENT-IDENTIFIER: US 5901301 A

TITLE: Data processor and method of processing data

DATE-ISSUED: May 4, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Matsuo; Masahito	Tokyo	N/A	N/A	JPX
Yoshida; Toyohiko	Tokyo	N/A	N/A	JPX

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	Tokyo	N/A	N/A	JPX	03

APPL-NO: 8/ 699944
DATE FILED: August 20, 1996

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	8-021453	February 7, 1996

INT-CL: [6] G06F 9/30
US-CL-ISSUED: 395/388; 395/800.01
US-CL-CURRENT: 712/212; 712/1
FIELD-OF-SEARCH: 395/800.24, 395/800.01, 395/800.35, 395/800.41, 395/376, 395/382, 395/378, 395/386, 395/388, 395/391

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5201039	April 1993	Sakamura	711/201
☐	5481734	January 1996	Yoshida	395/566
☐	5485629	January 1996	Dulong	395/800
☐	5530817	June 1996	Masubuchi	395/375
☐	5630083	May 1997	Carbine	395/388
☐	5664136	September 1997	Witt	395/338

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY
0 427 245 A2	May 1991	EPX
53-44130	April 1978	JPX
57-113144	July 1982	JPX
60-134938	July 1985	JPX
60-138640	July 1985	JPX

OTHER PUBLICATIONS

Masaitsu Nakajima, Hiraku Nakano, Yasuhiro Nakakuru Tadahiro Yoshida Yoshiyuki Goi, Yuji Nakai, Reiji Segawa, Takashi Kishida, Hiroshi Kadota, Semiconductor Research Center, Matsushita electric Industrial Co., Ltd. OHMEGA: A VLSI Superscalar Processor Architecture for Numerical Applications 8345 Computer Architecture News, 18.sup.th Ann. Int. Symp. Computer Architecture, 19 (1991) May, No. 3, New York, US pp. 160-168.
Atsuchi Inoue and Kenji Takeda, Toshiba Corporation R&D Center Performance Evaluation for Variouss Configuration of Superscalar Processors 8345 Computer Architecture News 21(1993) Mar., No. 1, New York, US pp. 4-11.
Erdem Hokenek, member IEEE, Robert K. Motoye, member IEEEE, and Peter W. Cook, member IEEEE Second-Generation RISC Floating Point with Mulitply-Add Fused 8107 IEEE Journal of Solid-State Circuits, 25(1990) Oct., No. 5, New York, US pp. 1207-1212.
Kouhei Nadahara, Ichiro Kuroda, Masayuji Daito, Takashi Nakayama, NEC Corporation Low-Power Multimedia RISC 8207 IEEE Micro, 15(1995) Dec., No. 6, Los Alamito, CA, US pp. 20-29.
Lewis C. Eggebrecht, SAMS, pp. 59 to 62 and 67 to 68, "Interfacing to the IBM Personal Computer", 1990.

ART-UNIT: 273
PRIMARY-EXAMINER: Coleman; Eric
ATTY-AGENT-FIRM: Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

ABSTRACT:

A second decoder (114) of an instruction decode unit (119) decodes an operation code for a multiply-add operation, and a second operation unit (117) receives two data stored in a register file (115) to perform the multiply-add operation. In parallel with the operations of the second decoder (114) and the second operation unit (117), a first decoder (113) of the instruction decode unit (119) decodes an operation code for 2 data load, and an operand access unit (104) causes two data (e.g., n bits each) stored in an internal data memory (105) to be transferred in parallel in the form of combined 2n-bit data to a first operation unit (116). Then, two predetermined registers of the register file (115) store the respective n-bit data from the first operation unit (116).

28 Claims, 56 Drawing figures

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Search Results -

Term	Documents
ALU.USPT.	8433
DECODER.USPT.	73371
(2 AND ALU AND DECODER).USPT.	53

Database: US Patents Full-Text Database
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EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Refine Search: l2 and alu and decoder

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Search History

Today's Date: 9/28/2000

DB Name	Query	Hit Count	Set Name
USPT	l2 and alu and decoder	53	L4
USPT	l1 and (yoshida.in. and fujii.in.)	10	L3
USPT	l1 and (yoshida.in. or fujii.in.)	753	L2
USPT	mitsubishi.asn.	23376	L1

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L11: Entry 3 of 12 File: USPT Oct 27, 1998

DOCUMENT-IDENTIFIER: US 5828886 A
TITLE: Compiling apparatus and method for promoting an optimization effect of a program

DEPR:
Entered in the architecture information table 21 is architecture information such as the number of available registers, instruction sets, instruction latency indicating the instruction delay, etc., for the computer in which a program to be compiled is executed. In the example shown in FIG. 3, the number of registers is 32 for both general-purpose registers and floating point registers. Set in the instruction set column is information for use in converting instructions into standardized internal instructions, for example, an add instruction into an internal operation code INST.sub.13 ADD, an addl instruction into an internal operation code INST.sub.13 ADD.sub.-- L, etc. Entered in the instruction latency column is instruction delay in the four cases where two instructions are not dependent on each other; two instructions are definition-reference related; two instructions are reference-definition related; and two instructions are definition-definition related. In this example, the delay of an add instruction and an addl instruction is represented by 1, and the delay of a dependent fadd instruction (floating point add instruction) is represented by 4. Other information about the number and types of operating units, etc. is entered in the architecture information table 21.

WEST

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L11: Entry 3 of 12 File: USPT Oct 27, 1998

US-PAT-NO: 5828886
DOCUMENT-IDENTIFIER: US 5828886 A

TITLE: Compiling apparatus and method for promoting an optimization effect of a program

DATE-ISSUED: October 27, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hayashi; Masakazu	Kawasaki	N/A	N/A	JPX

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Fujitsu Limited	Kawasaki	N/A	N/A	JPX	03

APPL-NO: 8/ 393561
DATE FILED: February 23, 1995

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	06-025171	February 23, 1994

INT-CL: [6] G06F 9/45
US-CL-ISSUED: 395/709; 395/707
US-CL-CURRENT: 717/9
FIELD-OF-SEARCH: 395/700, 395/705, 395/707, 395/709

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4931928	June 1990	Greenfeld	395/708
☐	5021945	June 1991	Morrison et al.	395/375
☐	5261062	November 1993	Sato	395/705
☐	5404551	April 1995	Katsuno	395/800
☐	5428793	June 1995	Odnert et al.	395/709
☐	5497499	March 1996	Garg et al.	395/393
☐	5557793	September 1996	Senter et al.	395/614

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY
2-257224	October 1990	JPX
5265769	October 1993	JPX
5-265769	October 1993	JPX

OTHER PUBLICATIONS

Vias et al., "Snooper," Ver 3, ref. man., Vias and Assoc., pp. 26-31, Jan. 1989.
Johnson, Mike "Superscalar Microprocessor Design" Prentice-Hall pp. 9-30, 103-146 Jan. 1991.
Vias et al. "SNOOPER" Version 3 reference manual Vias and Associates pp. 26-31, Jan. 1989.

ART-UNIT: 274
PRIMARY-EXAMINER: Voeltz; Emanuel Todd
ASSISTANT-EXAMINER: Corcoran, III; Peter J.
ATTY-AGENT-FIRM: Staas & Halsey

ABSTRACT:

A compiling apparatus and method in which instructions are scheduled for an efficient parallel process with a register allotting process and an instruction scheduling process performed independently of each other. An instruction scheduling unit collects information indicating the range of available registers, and renames registers by replacing the register numbers used by the instructions with other register numbers according to the collected register information and the analysis of definition/reference instruction dependency. The instructions are scheduled after the registers have been renamed.

13 Claims, 27 Drawing figures

WEST

Generate Collection

L1: Entry 1 of 12 File: USPT Mar 7, 2000

US-PAT-NO: 6035389
DOCUMENT-IDENTIFIER: US 6035389 A

TITLE: Scheduling instructions with different latencies

DATE-ISSUED: March 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Grochowski; Edward	San Jose	CA	N/A	N/A
Mulder; Hans	San Francisco	CA	N/A	N/A
Lin; Derrick C.	Foster City	CA	N/A	N/A

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA	N/A	N/A	02

APPL-NO: 9/ 132043
DATE FILED: August 11, 1998

INT-CL: [7] G06F 9/38
US-CL-ISSUED: 712/216; 712/215, 712/217
US-CL-CURRENT: 712/216; 712/215, 712/217
FIELD-OF-SEARCH: 712/215, 712/216, 712/217

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5404469	April 1995	Chung et al.	712/215
☐	5657315	August 1997	Waclawsky	370/452
☐	5745724	April 1998	Favor et al.	712/213
☐	5828868	October 1998	Sager et al.	713/501

ART-UNIT: 273
PRIMARY-EXAMINER: Treat; William M.
ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman LLP

ABSTRACT:

An apparatus includes a clock to produce pulses and an electronic hardware structure having a plurality of rows and one or more ports. Each row is adapted to record a separate latency vector written through one of the ports. The latency vector recorded therein is responsive to the clock. A method of dispatching instructions in a processor includes updating a plurality of expected latencies to a portion of rows of a register latency table, and decreasing the expected

a portion of rows of a register latency table, and decreasing the expected latencies remaining in other of the rows in response to a clock pulse. The rows of the portion correspond to particular registers.

47 Claims, 9 Drawing figures

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L2: Entry 4 of 4 File: USPT Apr 4, 1995

US-PAT-NO: 5404469
DOCUMENT-IDENTIFIER: US 5404469 A

TITLE: Multi-threaded microprocessor architecture utilizing static interleaving

DATE-ISSUED: April 4, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chung; Jin-Chin	Hsinchu	N/A	N/A	TWX
Wu; Chuan-Lin	Austin	TX	N/A	N/A

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Industrial Technology Research Institute	Hsinchu	N/A	N/A	TWX	03

APPL-NO: 7/ 840903
DATE FILED: February 25, 1992

INT-CL: [6] G06F 9/24, G06F 9/30, G06F 9/38
US-CL-ISSUED: 395/375; 364/231.8, 364/948.34
US-CL-CURRENT: 712/215; 711/119, 711/125, 717/6
FIELD-OF-SEARCH: 395/375, 395/800

REF-CITED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5226125	July 1993	Balmer	395/325

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY
0433864	June 1991	EPX

OTHER PUBLICATIONS

"Distributed Instruction Set Computer Architecture", IEEE Trans. on Computer, 1991, L. Wang and C. L. Wu.
"A Benchmark Evaluation of a Multi-threaded RISC Porcessor Architecture", Proc, of the International Conference on Parallel Processing, 1991, R. G. Prasadh and C. L. Wu.
"Computer Architecture and Parallel Processing" by Kai Hwang & Faye A. Briggs, 1984, McGraw-Hill, Inc, pp. 20-40.

ART-UNIT: 235

PRIMARY-EXAMINER: Eng; David Y.
ATTY-AGENT-FIRM: Meltzer, Lippe, Goldstein, Wolf, Schlissel & Sazer

ABSTRACT:

A static interleaving technique solves the problem of resource contention in a very long instruction word multi-threaded microprocessor architecture. In the static interleaving technique, each function unit in the processor is allocated for the execution of an instruction from a particular thread in a fixed predetermined time slot in a repeating pattern of predetermined time slots. The fixed predetermined pattern of time slots represents the resource constraints imposed on the hardware to resolve the contention for computing resources among the instruction threads. The strategy of resource allocation is exposed to a parallel compiler which organizes a sequence of instructions into the horizontal instruction words which form each thread so as to maintain the data dependencies among the instructions and to take into account the fixed predetermined allocation of hardware resources.

11 Claims, 16 Drawing figures

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INTEL.UG71,UG72,UG73,UG74,UG75,UG76,UG77,UG78,UG79,UG80,UG81,UG82,UG83,UG84,UG
REGISTER$1
REGISTER.USPT.
REGISTERA.USPT.
REGISTERB.USPT.
REGISTERC.USPT.
REGISTERD.USPT.
REGISTERE.USPT.
REGISTERF.USPT.
REGISTERL.USPT.
(INTEL.AS. AND (REGISTER$1 NEAR DELAY)).USPT.

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DB Name	Query	Hit Count	Set Name
USPT	intel.as. and (register$1 near delay)	7	L9
USPT	intel.as. and register$1 near delay	7	L8
USPT	patel.xa. and intel.asn. and delay	2	L7
USPT	l5 and branch$3	0	L6
USPT	6035389.pn.	1	L5
USPT	6035389.uref.	0	L4
USPT	6035389	1	L3
USPT	(5404469| 5657315| 5745724| 5828868)![pn]	4	L2
USPT	treat.xp. and intel.as. and delay	12	L1

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L11: Entry 1 of 18 File: USPT Apr 25, 2000

DOCUMENT-IDENTIFIER: US 6055626 A
TITLE: Method and circuit for delayed branch control and method and circuit for conditional-flag rewriting control

BSPR:
A skilled programmer who has better knowledge of delayed branch would make a proper modification to the program by inserting a no-operate (NOP) instruction between the consecutive delayed branch instructions with a view to avoiding the problem. However, since the modification is troublesome, it is forgotten many a time. Moreover, if the processor has an increased number of delay slots, it is necessary to insert as many no-operate instructions as the delay slots, so that the program becomes redundant and the memory capacity for storing the program is increased accordingly.

CCOR:
712/216

WEST

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L11: Entry 1 of 18 File: USPT Apr 25, 2000

US-PAT-NO: 6055626
DOCUMENT-IDENTIFIER: US 6055626 A

TITLE: Method and circuit for delayed branch control and method and circuit for conditional-flag rewriting control

DATE-ISSUED: April 25, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yasoshima; Hiroyuki	Menlo Park	CA	N/A	N/A
Kabuo; Hideyuki	Osaka	N/A	N/A	JPX

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Matsushita Electric Industrial Co., Ltd.	Osaka	N/A	N/A	JPX	03

APPL-NO: 9/ 120276
DATE FILED: July 22, 1998

PARENT-CASE:
This is a divisional application of Ser. No. 08/865,160, filed May 29, 1997 .

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	8-136212	May 30, 1996

INT-CL: [7] G06F 9/38
US-CL-ISSUED: 712/216; 712/217, 712/234
US-CL-CURRENT: 712/216; 712/217, 712/234
FIELD-OF-SEARCH: 712/216, 712/217, 712/233, 712/234

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3760365	September 1973	Kurtzberg et al.	712/216
☐	5471593	November 1995	Branigin	N/A
☐	5487156	January 1996	Popescu et al.	712/217

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY
62-147530	July 1987	JPX
3-122718	May 1991	JPX
4-127237	April 1992	JPX

OTHER PUBLICATIONS

Sun Microsystems Inc., "Spark Architecture Manual", The SPARC Architecture Manual, Version 8, Jan. 30, 1991, pp. 43-48.
J. Cortadella et al.: "Designing a Branch Target Buffer for Executing Branches With Zero Time Cost in a RISC Processor", Microprocessing & Microprogramming, vol. 24, No. 1-6, Aug, 1988, pp. 573-580, XP000038090.
A.M. Gonzalez: "A survey of branch techniques in pipelined processors" Microprocessing & Microprogamming, vol. 36, No. 5, Oct. 1993, pp. 243-257, XP000397907.
M. J. Mahom et al: "Hewlett-Packard Precision Architecture: The Processor" Hewlett-Packard Journal, vol. 37, No. 8, Aug. 1986, pp. 4-21, XP000211314.
G.B. Steven, et al., "ALU Design and processor branch architecture" Microprocessing and Microprogramming, vol. 36, No. 5, Oct. 1993, Amsterdam, NL, pp. 259-278.
J.A. Derosa, et al., "An Evaluation of Branch Architectures", Proceedings fo the 14th Annual International Symposium of Computer Architecture, Jun. 2-5, 1987, Pittsburgh, PA, US, pp. 10-16.

ART-UNIT: 273
PRIMARY-EXAMINER: Treat; William M.
ATTY-AGENT-FIRM: McDermott, Will & Emery

ABSTRACT:

In a processor employing a delayed branch method, delayed branch control which does not complicate instruction execution sequence and improves the readability of a program on the assembler level is implemented without providing a control bit in an instruction code. The delayed branch control according to the present invention involves the use of a branch-information storing circuit for storing the occurrence or nonoccurrence of a branch in a specified one of a continuous sequence of cycles immediately before a current execute cycle which are equal in number to delay slots in the processor. In executing a delayed branch instruction, when the branch-information storing circuit stores the occurrence of a branch in the specified cycle, a branch is disabled. This prevents instruction execution sequence from being complicated even when individual branch conditions for consecutive delayed branch instructions are satisfied, so that the program on the assembler level is improved in readability. The branch-information storing circuit can simply be composed of a combination of a shift register, a counter, and a latch.

6 Claims, 17 Drawing figures

WEST

Generate Collection

L11: Entry 3 of 18 File: USPT Nov 16, 1999

US-PAT-NO: 5987594
DOCUMENT-IDENTIFIER: US 5987594 A

TITLE: Apparatus for executing coded dependent instructions having variable latencies

DATE-ISSUED: November 16, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Panwar; Ramesh	Santa Clara	CA	N/A	N/A
Hetherington; Ricky C.	Pleasanton	CA	N/A	N/A

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Palo Alto	CA	N/A	N/A	02

APPL-NO: 8/ 881726
DATE FILED: June 25, 1997

PARENT-CASE:
The subject matter of the present application is related to that of U.S. patent application Ser. No. 08/881,958, now U.S. Pat. No. 5,826,765 identified as Docket No. P2345/37178.830071.000 for AN APPARATUS FOR HANDLING ALIASED FLOATING-POINT REGISTERS IN AN OUT-OF-ORDER PROCESSOR filed concurrently herewith by Ramesh Panwar; Ser. No. 08/881,729 identified as Docket No. P2346/37178.830072.000 for APPARATUS FOR PRECISE ARCHITECTURAL UPDATE IN AN OUT-OF-ORDER PROCESSOR filed concurrently herewith by Ramesh Panwar and Arjun Prabhu; Ser. No. 08/881,726 identified as Docket No. P2348/37178.830073.000 for AN APPARATUS FOR NON-INTRUSIVE CACHE FILLS AND HANDLING OF LOAD MISSES filed concurrently herewith by Ramesh Panwar and Ricky C. Hetherington; Ser. No. 08/881,908 identified as Docket No. P2349/37178.830074.000 for AN APPARATUS FOR HANDLING COMPLEX INSTRUCTIONS IN AN OUT-OF-ORDER PROCESSOR filed concurrently herewith by Ramesh Panwar and Dani Y. Dakhil; Ser. No. 08/882,173, now U.S. Pat. No. 5,898,853 identified as Docket No. P2350/37178.830075.000 for AN APPARATUS FOR ENFORCING TRUE DEPENDENCIES IN A N OUT-OF-ORDER PROCESSOR filed concurrently herewith by Ramesh Panwar and Dani Y. Dakhil; Ser. No. 08/881,145 identified as Docket No. P2351/37178.830076.000 for APPARATUS FOR DYNAMICALLY RECONFIGURING A PROCESSOR filed concurrently herewith by Ramesh Panwar and Ricky C. Hetherington; Ser. No. 08/881,732 identified as Docket No. P2353/37178.830077.000 for APPARATUS FOR ENSURING FAIRNESS OF SHARED EXECUTION RESOURCES AMONGST MULTIPLE PROCESSES EXECUTING ON A SINGLE PROCESSOR filed concurrently herewith by Ramesh Panwar and Joseph I. Chamdani; Ser. No. 08/882,175 identified as Docket No. P2355/37178.830078.000 for SYSTEM FOR EFFICIENT IMPLEMENTATION OF MULTI-PORTED LOGIC FIFO STRUCTURES IN A PROCESSOR filed concurrently herewith by Ramesh Panwar; Ser. No. 08/882,311 identified as Docket No. P2365/37178.830080.000 for AN APPARATUS FOR MAINTAINING PROGRAM CORRECTNESS WHILE ALLOWING LOADS TO BE BOOSTED PAST STORES IN AN OUT-OF-ORDER MACHINE filed concurrently herewith by Ramesh Panwar, P. K. Chidambaran and Ricky C. Hetherington; Ser. No. 08/881,731 identified as Docket No. P2369/37178.830081.000 for APPARATUS FOR TRACKING PIPELINE RESOURCES IN A SUPERSCALAR PROCESSOR filed concurrently herewith by Ramesh Panwar; Ser. No. 08/882,525 identified as Docket No. P2370/37178.830082.000 for AN APPARATUS FOR RESTRAINING OVER-EAGER LOAD BOOSTING IN AN OUT-OF-ORDER MACHINE filed concurrently herewith by Ramesh Panwar and Ricky C. Hetherington; Ser. No. 08/882,220 identified as Docket No.

DB Name	Query	Hit Count	Set Name
USPT	4792892.uref.	18	L22
USPT	4792892.pn.	1	L21
USPT	delay field near instruction$1	6	L20
JPAB,EPAB,DWPI,TDBD	113 near2 instruction$1	1	L19
JPAB,EPAB,DWPI,TDBD	113 near macroinstruction$1	0	L18
JPAB,EPAB,DWPI,TDBD	113 near macro-instruction$1	0	L17
JPAB,EPAB,DWPI,TDBD	113 near micro-instruction$1	0	L16
JPAB,EPAB,DWPI,TDBD	113 near microinstruction$1	0	L15
JPAB,EPAB,DWPI,TDBD	113 near instruction$1	1	L14
JPAB,EPAB,DWPI,TDBD	delay field	84	L13
JPAB,EPAB,DWPI,TDBD	(register$1 near delay) and instruction$1	32	L12
USPT	110 and (instruction$1 near delay)	18	L11
USPT	(712/216)!.CCLS. or 712.222.ccls.	234	L10
USPT	intel.as. and (register$1 near delay)	7	L9
USPT	intel.as. and register$1 near delay	7	L8
USPT	patel.xa. and intel.asn. and delay	2	L7
USPT	15 and branch$3	0	L6
USPT	6035389.pn.	1	L5
USPT	6035389.uref.	0	L4
USPT	6035389	1	L3
USPT	(5404469| 5657315| 5745724| 5828868)![pn]	4	L2
USPT	treat.xp. and intel.as. and delay	12	L1

WEST

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Search Results -

Term	Documents
INSTRUCTION$1	0
INSTRUCTION.USPT.	72829
INSTRUCTIONG.USPT.	3
INSTRUCTIONJ.USPT.	1
INSTRUCTIONN.USPT.	2
INSTRUCTIONS.USPT.	98901
INSTRUCTION1.USPT.	2
INSTRUCTION2.USPT.	1
INSTRUCTION3.USPT.	1
INSTRUCTION+.USPT.	1
(L10 AND (INSTRUCTION$1 NEAR DELAY)).USPT.	18

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Database: US Patents Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Refine Search: Clear

Search History

Today's Date: 9/28/2000

DB Name	Query	Hit Count	Set Name
USPT	l10 and (instruction$1 near delay)	18	L11
USPT	(712/216)!.CCLS. or 712.222.ccls.	234	L10
USPT	intel.as. and (register$1 near delay)	7	L9
USPT	intel.as. and register$1 near delay	7	L8
USPT	patel.xa. and intel.asn. and delay	2	L7
USPT	l5 and branch$3	0	L6
USPT	6035389.pn.	1	L5
USPT	6035389.uref.	0	L4
USPT	6035389	1	L3
USPT	(5404469| 5657315| 5745724| 5828868)![pn]	4	L2
USPT	treat.xp. and intel.as. and delay	12	L1

WEST

Generate Collection

L12: Entry 5 of 32 File: JPAB Oct 2, 1987

PUB-NO: JP362224817A
DOCUMENT-IDENTIFIER: JP 62224817 A
TITLE: DATA PROCESSOR

PUBN-DATE: October 2, 1987

INVENTOR-INFORMATION:
NAME
IIDA, KOICHI

ASSIGNEE-INFORMATION:
NAME COUNTRY
HITACHI LTD N/A

APPL-NO: JP61065735
APPL-DATE: March 26, 1986

INT-CL (IPC): G06F 1/02; G06F 7/60; G06F 9/34; G06F 12/00

ABSTRACT:

PURPOSE: To contrive the effective use of data supplied to a delay register by providing a delay register that holds input data and supplying the held data selectively to a data memory.

CONSTITUTION: Data read out from a data memory DM are always supplied to a delay register DR regardless of the content of arithmetic processing. Supplied data are held until succeeding arithmetic process instruction executing cycle even when a succeeding instruction execution cycle is a transfer instruction execution cycle or jump instruction execution cycle. The held data are made writable in the memory DM in succeeding arithmetic process instruction execution cycle. Thus, data supplied to the register DR can be utilized effectively, and at the same time, the high speed processing of data and reduction of the number of program steps can be realized.

WEST

Generate Collection

L12: Entry 18 of 32 File: DWPI Aug 25, 1993

DERWENT-ACC-NO: 1993-266170
DERWENT-WEEK: 199334

TITLE: Latching system for microinstruction based processors - includes additional microinstruction delay register between the selector and decoder circuits and controls third data bus and registers

INVENTOR: KUSUDA, M

PATENT-ASSIGNEE:

ASSIGNEE	CODE
NEC CORP	NIDE

PRIORITY-DATA:
1992JP-0029822 February 18, 1992

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 556825 A1	August 25, 1993	E	017	G06F009/28

DESIGNATED-STATES: DE FR GB

CITED-DOCUMENTS:01Jnl.Ref; EP 388735 ; GB 2115964 ; JP58213352

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	APPL-DESCRIPTOR
EP 556825A1	February 18, 1993	1993EP-0102559	N/A

INT-CL (IPC): G06F 9/28

ABSTRACTED-PUB-NO: EP 556825A
BASIC-ABSTRACT:

The microinstruction based processor includes a ROM(102) supplying microinstructions to a selector(104) with a repeat register(103). A control circuit(107) for the partial instruction selector(106). Instructions are fed from this selector to a decoder(109) partly through an instruction delay register(108). The instruction is then executed in the operating section(110).

One field(212) from the microinstruction controls two data buses and a group of registers directly. The field from the delay register controls a third data bus and register, and the operating code is delayed by one cycle.

ADVANTAGE - Reduces the number of cycles required to perform instructions and also reduces the number of registers required.

DD

ABSTRACTED-PUB-NO: EP 556825A
EQUIVALENT-ABSTRACTS:

CHOSEN-DRAWING: Dwg.9/12

DERWENT-CLASS: T01
EPI-CODES: T01-F01; T01-M06A;

WEST

Generate Collection

L12: Entry 31 of 32 File: DWPI Nov 30, 1981

DERWENT-ACC-NO: 1982-M9138E
DERWENT-WEEK: 198239

TITLE: Interrupt analyser for multi-program computers - has extra registers and delay elements for executing instructions preceding interruption generating instruction

INVENTOR: ABUZYAROV, V M

PATENT-ASSIGNEE:

ASSIGNEE	CODE
ABUZYAROV V M	ABUZI

PRIORITY-DATA:
1979SU-2837250 November 22, 1979

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
SU 886000 B	November 30, 1981	N/A	006	N/A

INT-CL (IPC): G06F 9/46

ABSTRACTED-PUB-NO: SU 886000B
BASIC-ABSTRACT:

The analyser is designed for use in both universal and specialised digital computers.

A register (15) stores the address of the preceding instruction in the case of an interruption, whilst a counter (19) stores the address of the current instruction. If the latter causes disruption of the normal instruction sequence, its address is fed into a local memory (10). A signal from a delay element (20) increases the contents of the counter by 1 and is also fed to a 2nd delay element (21), which causes the contents of a program state register (6) to be fed into a buffer (15) and also energises a shift register (14), which shifts the instruction length code from the program state register, a jump sign, and an interruption sign.

When an instruction which caused an interruption is executed, the interrupt signals are fed by an OR element (16) to the jump sign register (13), and the address of this instruction is stored in the buffer for the whole of the duration of the interruption. Bul.44/30.11 .81

ABSTRACTED-PUB-NO: SU 886000B
EQUIVALENT-ABSTRACTS:

CHOSEN-DRAWING: Dwg.1/1

DERWENT-CLASS: T01
EPI-CODES: T01-F02;

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Search Results -

Term	Documents
REGISTER$1	0
REGISTER.DWPI,TDBD,EPAB,JPAB.	201019
REGISTERA.DWPI,TDBD,EPAB,JPAB.	1
REGISTERD.DWPI,TDBD,EPAB,JPAB.	61
REGISTERE.DWPI,TDBD,EPAB,JPAB.	23
REGISTERI.DWPI,TDBD,EPAB,JPAB.	3
REGISTERK.DWPI,TDBD,EPAB,JPAB.	1
REGISTERO.DWPI,TDBD,EPAB,JPAB.	1
REGISTERR.DWPI,TDBD,EPAB,JPAB.	1
REGISTERS.DWPI,TDBD,EPAB,JPAB.	69137
((REGISTER$1 NEAR DELAY) AND INSTRUCTION$1).JPAB,EPAB,DWPI,TDBD.	32

There are more results than shown above. Click here to view the entire set.

Database: US Patents Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Refine Search: (register$1 near delay) and instruction$1 Clear

Search History

Today's Date: 9/28/2000

DB Name	Query	Hit Count	Set Name
JPAB,EPAB,DWPI,TDBD	(register$1 near delay) and instruction$1	32	L12
USPT	110 and (instruction$1 near delay)	18	L11
USPT	(712/216)!.CCLS. or 712.222.ccls.	234	L10
USPT	intel.as. and (register$1 near delay)	7	L9
USPT	intel.as. and register$1 near delay	7	L8
USPT	patel.xa. and intel.asn. and delay	2	L7
USPT	15 and branch$3	0	L6
USPT	6035389.pn.	1	L5
USPT	6035389.uref.	0	L4
USPT	6035389	1	L3
USPT	(5404469| 5657315| 5745724| 5828868)![pn]	4	L2
USPT	treat.xp. and intel.as. and delay	12	L1

WEST

End of Result Set

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L14: Entry 1 of 1 File: DWPI Aug 7, 1985

DERWENT-ACC-NO: 1985-191546
DERWENT-WEEK: 198532

TITLE: Loop instruction data processor - uses counter, address register, program counter, clock, ROM, instruction register and loop counter

ABEQ:
A processor for treating data, comprising: a programme memory (1) for storing a plurality of instructions, including a programme loop control instruction which is defined by an intial address and a final address and which comprises a repetition field for defining the desired number of loop repeats, a programme counter (5) with a first step-wise control for applying the addresses to said programme memory, loop counting means (35) for counting the number of loop repeats after each passage of the initial address, a first register (30) for storing said initial address, first detection means for detecting the appearance of the final address in order to load the programme counter with the contents of said first register, second detection means which are coupled to said counting means and which operate as a function of the repetition field so as to inhibit said first detection means upon the appearance of the desired number of repeats in order to enable the programme counter to abandon said programme loop, characterised in that the control instruction also comprises a delay field for defining an addressing interval between the control instruction and said initial address, and in that for treating said delay field the processor comprises: a delay counter (50) which is loaded as a function of the delay field with a second control for operation in synchronism with said programme counter during the delay interval, third detection means which are coupled to said delay counter so as to detect the end of the delay interval and to load said first register. (8pp)

WEST

End of Result Set

Generate Collection

L14: Entry 1 of 1 File: DWPI Aug 7, 1985

DERWENT-ACC-NO: 1985-191546
DERWENT-WEEK: 198532

TITLE: Loop instruction data processor - uses counter, address register, program counter, clock, ROM, instruction register and loop counter

INVENTOR: BARAZESH, B; MARY, L

PATENT-ASSIGNEE:

ASSIGNEE	CODE
TRT TELECOM RADIOELEC TEL SA	TRTT

PRIORITY-DATA:
1983FR-0021104 December 30, 1983

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 150535 A	August 7, 1985	F	013	N/A
DE 3482063 G	May 31, 1990	N/A	000	N/A
EP 150535 B	April 25, 1990	N/A	000	N/A
FR 2557712 A	July 5, 1985	N/A	000	N/A
US 4792892 A	December 20, 1988	N/A	000	N/A

DESIGNATED-STATES: DE FR GB IT SE DE FR GB IT SE

CITED-DOCUMENTS:2.Jnl.Ref; No-SR.Pub

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	APPL-DESCRIPTOR
EP 150535A	December 17, 1984	1984EP-0201883	N/A
US 4792892A	May 1, 1987	1987US-0048481	N/A

INT-CL (IPC): G06F 9/40

ABSTRACTED-PUB-NO: EP 150535A
BASIC-ABSTRACT:

Program instructions from a read-only memory (1) are passed to an instruction register (2) and control circuit (3). Address codes are generated by a program counter (5) which is stepped by a clock (10). A loop circuit (20) causes part of the program announced by a loop command instruction to be carried out by repeated execution of a sequence of instructions.

An instruction counter (25) provides an end-of-sequence signal which makes an instruction address register (30) recall from the program counter the address of the first instruction of the sequence. A loop counter (35) counts the number of executions of the sequence, and signals the end of that part of the program.

ADVANTAGE - Execution of looped sequence is not conditioned by absolute addresses

of instructions.

ABSTRACTED-PUB-NO: EP 150535B
EQUIVALENT-ABSTRACTS:

A processor for treating data, comprising: a programme memory (1) for storing a plurality of instructions, including a programme loop control instruction which is defined by an intial address and a final address and which comprises a repetition field for defining the desired number of loop repeats, a programme counter (5) with a first step-wise control for applying the addresses to said programme memory, loop counting means (35) for counting the number of loop repeats after each passage of the initial address, a first register (30) for storing said initial address, first detection means for detecting the appearance of the final address in order to load the programme counter with the contents of said first register, second detection means which are coupled to said counting means and which operate as a function of the repetition field so as to inhibit said first detection means upon the appearance of the desired number of repeats in order to enable the programme counter to abandon said programme loop, characterised in that the control instruction also comprises a delay field for defining an addressing interval between the control instruction and said initial address, and in that for treating said delay field the processor comprises: a delay counter (50) which is loaded as a function of the delay field with a second control for operation in synchronism with said programme counter during the delay interval, third detection means which are coupled to said delay counter so as to detect the end of the delay interval and to load said first register. (8pp)

US 4792892A

To execute a loop control instruction, calling for repeated execution N times of a sequence of "i" instructions, the processor includes a loop circuit. The circuit comprises an instruction counter which counts execution of the instructions in the loop sequence and produces an end-of-sequence signal upon each completion of the loop.

A register refreshes the program counter with the address of the first instruction in the loop in response to each end-of-sequence signal.

A loop counter counts the number of completions of the loop and delivers a signal indicating the end of loop portion of the entire program and enables the program counter to continue with the rest the program. The delay in loop execution permits initialising of registers in the data processor to permit pipeline execution of the loop instruction.

ADVANTAGE - Synchronisation problems are avoided.

CHOSEN-DRAWING: Dwg.1/5 Dwg.1/5y

DERWENT-CLASS: T01
EPI-CODES: T01-F09;

WEST

Generate Collection

L20: Entry 1 of 6 File: USPT Jun 9, 1998

DOCUMENT-IDENTIFIER: US 5765037 A
TITLE: System for executing instructions with delayed firing times

DEPR:
The delay unit 1940 determines the amount of time that instruction fetching can be continued after the receipt of a branch instruction by the BEU. Previously, it has been described that when a branch instruction is received by the BEU, instruction fetching continues for one more cycle and then stops. The instruction fetched during this cycle is held up from passing through PIQ bus interface unit 1544 until the length of the delay field has been determined. For example, if the delay field is zero (implying that the branch is to be executed immediately), these instructions must still be withheld from the PIQ bus buffer unit until it is determined whether or not these are the right instructions to be fetched. If the delay field is non-zero, the instructions would be gated into the PIQ buffer unit as soon as the delay value was determined to be non-zero. The length of the delay is obtained from DELAY field of the instruction register 1900. The delay unit receives the delay length from register 1900 and clock impulses from the context control 1518 over lines 1549. The delay unit 1940 decrements the value of the delay at each clock pulse; and when fully decremented, the interface unit 1950 becomes enabled.

WEST

Generate Collection

L20: Entry 1 of 6 File: USPT Jun 9, 1998

US-PAT-NO: 5765037
DOCUMENT-IDENTIFIER: US 5765037 A

TITLE: System for executing instructions with delayed firing times

DATE-ISSUED: June 9, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Morrison; Gordon Edward	Denver	CO	N/A	N/A
Brooks; Christopher Bancroft	Boulder	CO	N/A	N/A
Gluck; Frederick George	Boulder	CO	N/A	N/A

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Biax Corporation	Palm Beach Gardens	FL	N/A	N/A	02

APPL-NO: 8/ 480841
DATE FILED: June 7, 1995

PARENT-CASE:
This is a divisional of U.S. Ser. No. 08/254,687, filed Jun. 6, 1994, now issued U.S. Pat. No. 5,517,628, which is a divisional of Ser. No. 08/093,794, filed Jul. 19, 1993, now abandoned, which is a continuation of Ser. No. 07/913,736, filed Jul. 14, 1992, now abandoned, which is a continuation of Ser. No. 07/560,093, filed Jul. 30, 1990, now abandoned, which is a divisional of Ser. No. 07/372,247, filed Jun. 26, 1989, now U.S. Pat. No. 5,021,945, which is a divisional of Ser. No. 06/794,221, filed Oct. 31, 1985, now U.S. Pat. No. 4,847,755.

INT-CL: [6] G06F 9/40
US-CL-ISSUED: 395/557; 395/391, 395/559, 395/800.21, 395/580
US-CL-CURRENT: 713/502; 712/21, 712/215, 712/233
FIELD-OF-SEARCH: 395/375, 395/550, 395/391, 395/595, 395/557, 395/559, 395/800.21, 395/580

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4200912	April 1980	Harrington et al.	395/742
☐	4229790	October 1980	Gilliland et al.	395/671
☐	4247894	January 1981	Beismann et al.	395/737
☐	4250546	February 1981	Boney et al.	395/735
☐	4342078	July 1982	Tredennick et al.	395/387
☐	4430707	February 1984	Kim	395/670
☐	4466061	August 1984	DeSantis	395/676
☐	4532589	July 1985	Shintani et al.	395/393
☐	4598400	July 1986	Hillis	370/400
☐	4833599	May 1989	Colwell et al.	395/583

OTHER PUBLICATIONS

Chang et al., "801 Storage: Architecture and Programming," IBM T.J. Watson Research Center, 1988, 0734-2071/88/0200-0028, pp. 29-50.
Colwell et al., "A VLIW Architecture for a Trace Scheduling Compiler," Second International Conference on ASPLOS-II, Oct. 5-8, 1987, pp. 1-23.
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Ellis, "Bulldog: A Compiler for VLIW Architectures," MIT, 1986.
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McDowell et al., "Processor Scheduling for Linearly Connected Parallel Processors," IEEE Transactions on Computers, 1986, 0018-9340/86/0700-0632, vol. C-35, No. 7, pp. 633-638.
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Tomita et al., "A User-Microprogrammable, Local Host Computer with Low-Level Parallelism," Communications of the ACM, 0149-7111/83/0600/0151, pp. 151-157, 1983.
Alpha Architecture Reference Manual, Digital, 1992.
PowerPC 601 RISC Microprocessor User's Manual, IBM, 1993.
Intel MCS-80 User's Manual, Intel, Oct. 1977.
Heinrich, MIPS Microprocessor R4000 User's Manual, MIPS Technologies, Inc., 1993.
MC68030 Enhanced 32-Bit Microprocessor User's Manual, Second Edition, Motorola, Inc., 1989.

ART-UNIT: 235

PRIMARY-EXAMINER: Kim; Kenneth S.
ATTY-AGENT-FIRM: Fish & Richardson P.C.

ABSTRACT:

A system and method reorder instructions for effecting faster branch execution. A processor element is coupled to receive stored instructions in a first order, and to process the received instructions in a different order, the processing occurring after each stored instruction of a first type is issued, and after a delay time, after each stored instruction of a second type is issued. The delay time is based on a delay value associated with the second type of instructions. In particular, the instructions include branch and non-branch instruction wherein firing time information identifies a time of execution of the branch instruction which is a variable number of instructions cycles prior to a time of execution of a last to be executed instruction in a basic block. Accordingly, branch instructions can be completely executed no later than during the processing of the last to be executed non-branch instruction in the basic block thereby speeding up overall processing of the software program by the system.

29 Claims, 27 Drawing figures

WEST

Generate Collection

L20: Entry 2 of 6 File: USPT Apr 14, 1998

DOCUMENT-IDENTIFIER: US 5740220 A
TITLE: Signal generating device including programmable counters and a programmable serial bit pattern generator

BSPR:
The invention relates to a microprocessor comprising registered counting means that have a clock input for under control of attainment of a predetermined clock count generating a command signal on a command signal output thereof. Various counting means have been described for use in a microprocessor, such as U.S. Ser. No. 07/048,841, filed May 1, 1987, now issued in U.S. Pat. No. -4,792,892. The reference relates to a microprocessor, wherein a program loop instruction has a delay field. Through this delay field, the actual start of the loop is delayed over a specified number of intervening instructions. After attaining the first loop instruction, both the number of instructions within a single execution of the loop and the number of successive executions of the loop are counted for so attaining a correct execution of the program. The present invention is not directed, however, to counting instructions.

WEST

End of Result Set

Generate Collection

L21: Entry 1 of 1 File: USPT Dec 20, 1988

US-PAT-NO: 4792892
DOCUMENT-IDENTIFIER: US 4792892 A

TITLE: Data processor with loop circuit for delaying execution of a program loop control instruction

DATE-ISSUED: December 20, 1988

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mary; Luc	Bures sur Yvette	N/A	N/A	FRX
Barazesh; Bahman	Paris	N/A	N/A	FRX

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Telecommunications Radioelectriques et Telephoniques T.R.T.	Paris	N/A	N/A	FRX	03

APPL-NO: 7/ 048461
DATE FILED: May 1, 1987

PARENT-CASE:
This is a continuation of application Ser. No. 682,227, filed Dec. 17, 1984, now abandoned.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
FR	83 21104	December 30, 1983

INT-CL: [4] G06F 9/40
US-CL-ISSUED: 364/200
US-CL-CURRENT: 712/241
FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3593306	July 1971	Toy	364/200
☐	3654613	April 1972	Dunne et al.	364/900
☐	3736567	May 1973	Lotan et al.	364/200
☐	4097920	June 1978	Ozga	364/200
☐	4562537	December 1985	Barnett et al.	364/200

OTHER PUBLICATIONS

I.B.M. Tech. Discl. Bull., vol. 14, No. 9, Feb. 1972, p. 2806.

ART-UNIT: 232
PRIMARY-EXAMINER: Zache; Raulfe B.
ASSISTANT-EXAMINER: Munteanu; Florin
ATTY-AGENT-FIRM: Briody; Thomas A. Haken; Jack E. Eason; Leroy

ABSTRACT:

A data processor for executing a program of instructions stored in a program memory controlled by a program counter. To execute a loop control instruction, calling for repeated execution N times of a sequence of "i" instructions, the processor includes a loop circuit having an instruction counter which counts execution of the instructions in the loop sequence and produces an end-of-sequence signal upon each completion of the loop, a register which refreshes the program counter with the address of the first instruction in the loop in response to each end-of-sequence signal, and a loop counter which counts the number of completions of the loop and delivers a signal indicating the end of the loop portion of the entire program and enabling the program counter to continue on with the rest of the program. The delay in loop execution permits initializing of registers in the data processor so as to permit pipeline execution of the loop instruction.

7 Claims, 5 Drawing figures

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Term	Documents
"4792892".USPT.	1
"4792892".PN..USPT.	1

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JPO Abstracts Database
EPO Abstracts Database
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Search History

Today's Date: 9/28/2000

DB Name	Query	Hit Count	Set Name
USPT	4792892.pn.	1	L21
USPT	delay field near instruction$1	6	L20
JPAB,EPAB,DWPI,TDBD	113 near2 instruction$1	1	L19
JPAB,EPAB,DWPI,TDBD	113 near macroinstruction$1	0	L18
JPAB,EPAB,DWPI,TDBD	113 near macro-instruction$1	0	L17
JPAB,EPAB,DWPI,TDBD	113 near micro-instruction$1	0	L16
JPAB,EPAB,DWPI,TDBD	113 near microinstruction$1	0	L15
JPAB,EPAB,DWPI,TDBD	113 near instruction$1	1	L14
JPAB,EPAB,DWPI,TDBD	delay field	84	L13
JPAB,EPAB,DWPI,TDBD	(register$1 near delay) and instruction$1	32	L12
USPT	110 and (instruction$1 near delay)	18	L11
USPT	(712/216)!.CCLS. or 712.222.ccls.	234	L10
USPT	intel.as. and (register$1 near delay)	7	L9
USPT	intel.as. and register$1 near delay	7	L8
USPT	patel.xa. and intel.asn. and delay	2	L7
USPT	15 and branch$3	0	L6
USPT	6035389.pn.	1	L5
USPT	6035389.uref.	0	L4
USPT	6035389	1	L3
USPT	(5404469| 5657315| 5745724| 5828868)![pn]	4	L2
USPT	treat.xp. and intel.as. and delay	12	L1

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L22: Entry 7 of 18 File: USPT May 12, 1998

US-PAT-NO: 5752015
DOCUMENT-IDENTIFIER: US 5752015 A

TITLE: Method and apparatus for repetitive execution of string instructions without branch or loop microinstructions

DATE-ISSUED: May 12, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Henry; Glenn	Austin	TX	N/A	N/A
Parks; Terry	Austin	TX	N/A	N/A

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Integrated Device Technology, Inc.	Santa Clara	CA	N/A	N/A	02

APPL-NO: 8/ 623657
DATE FILED: March 29, 1996

INT-CL: [6] G06F 9/30
US-CL-ISSUED: 395/588; 395/595
US-CL-CURRENT: 712/241; 712/245
FIELD-OF-SEARCH: 395/387, 395/588, 395/590, 395/595

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4449184	May 1984	Pohlman, III et al.	395/250
☐	4521858	June 1985	Kraemer et al.	395/421.05
☐	4652997	March 1987	Kloker	395/588
☐	4792892	December 1988	Mary et al.	395/588
☐	5404473	April 1995	Papworth et al.	395/588
☐	5507027	April 1996	Kawamoto	395/588

ART-UNIT: 274
PRIMARY-EXAMINER: Lall; Parshotam S.
ASSISTANT-EXAMINER: Vu; Viet
ATTY-AGENT-FIRM: Huffman; James W.

ABSTRACT:

An apparatus and method for improving the execution of string instructions is provided. The apparatus includes a translator which repetitively generates a micro instruction sequence applicable to the particular string operation to be performed, and an execution unit for executing the micro instruction sequence. In addition, a counter is provided to hold a count value corresponding to the number of times the micro instruction sequence is to be executed, and is decremented each time the sequence is executed. The translator continues to generate the micro instruction sequence until receiving a signal from a counter which indicates that all of the string has been operated upon. In addition, the execution unit receives the signal from the counter and tests subsequent micro instructions to determine whether they are associated with string instructions. If so, the execution unit performs NOPs in place of those micro instructions.

9 Claims, 6 Drawing figures

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L22: Entry 10 of 18 File: USPT Dec 10, 1996

US-PAT-NO: 5584031
DOCUMENT-IDENTIFIER: US 5584031 A

TITLE: System and method for executing a low power delay instruction

DATE-ISSUED: December 10, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Burch; Kenneth R.	Austin	TX	N/A	N/A
Feddeler; James R.	Austin	TX	N/A	N/A

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Motorola Inc.	Schaumburg	IL	N/A	N/A	02

APPL-NO: 8/ 407792
DATE FILED: March 20, 1995

PARENT-CASE:
This application is a continuation application Ser. No. 08/005,949, filed Jan. 19, 1993, now abandoned.

INT-CL: [6] G06F 1/32
US-CL-ISSUED: 395/750
US-CL-CURRENT: 713/323
FIELD-OF-SEARCH: 395/375, 395/550, 395/650, 395/750, 395/800

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3736569	May 1973	Bouricius et al.	340/172.2
☐	4203153	May 1980	Boyd	364/DIG.1
☐	4792892	December 1988	Mary et al.	395/375
☐	4875160	October 1989	Brown, III	395/375
☐	4958275	June 1990	Youkouchi	395/375
☐	5083266	January 1992	Watanabe	395/275

OTHER PUBLICATIONS

"M6805 HMOS M146805 CMOS Family Microcomputer/Microprocessor User's Manual", published by Motorola, Inc. in 1983, pp. 79-80, 83-87, 101-102, 211 and 219.
"M68HC11 Reference Manual" published by Motorola, Inc. in 1989, pp. A-74, 6-20; 3-1, 6-19, A-110 to A-111; 5-9, 5-21, A-93.

Computer Organization and Architecture, Principles of Structure and Function, 3rd Edition William Stallings, MacMillan Publishing Co., Pub. Sep. 1992 pp. 378, 468-471, 691.

ART-UNIT: 232
PRIMARY-EXAMINER: Donaghue; Larry D.
ATTY-AGENT-FIRM: Apperley; Elizabeth A.

ABSTRACT:

A system and method is provided for executing a low power no operation instruction in a data processor (10) with a minimal amount of power consumption. In the instruction, an opcode has a mnemonic form of "SLEEP" and an operand which specifies a number of timing cycles the instruction should be executed. During execution of the SLEEP instruction, the operand is provided to a general register (26) in a CPU (12) of the data processor (10). An ALU (28) accesses the register (26) and decrements the operand until the contents are equal to zero. When the ALU (28) has decremented the operand to zero, a next software instruction is accessed and executed by the data processor.

21 Claims, 2 Drawing figures

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L22: Entry 11 of 18 File: USPT Apr 9, 1996

US-PAT-NO: 5507027
DOCUMENT-IDENTIFIER: US 5507027 A

TITLE: Pipeline processor with hardware loop function using instruction address stack for holding content of program counter and returning the content back to program counter

DATE-ISSUED: April 9, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kawamoto; Koji	Itami	N/A	N/A	JPX

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	Tokyo	N/A	N/A	JPX	03

APPL-NO: 8/ 363114
DATE FILED: December 23, 1994

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	5-335377	December 28, 1993

INT-CL: [6] G06F 9/00, G06F 9/40
US-CL-ISSUED: 395/375; 364/231.8, 364/244.3, 364/251, 364/251.1, 364/259.2, 364/261.3, 364/262, 364/262.1, 364/262.4, 364/DIG.1
US-CL-CURRENT: 712/241
FIELD-OF-SEARCH: 395/375, 395/800, 395/725, 395/775, 395/200, 364/DIG.1

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3593306	July 1971	Toy et al.	395/375
☐	3736567	May 1973	Lotan et al.	395/775
☐	4097920	June 1978	Ozga	395/375
☐	4462074	July 1984	Linde	395/200
☐	4652997	March 1987	Kloker	395/375
☐	4792892	December 1988	Mary et al.	395/375
☐	4882701	November 1989	Ishii	395/375
☐	4910664	May 1990	Arizono	395/375
☐	5056004	October 1991	Ohde et al.	395/375
☐	5101484	March 1992	Kohn	395/375
☐	5303355	April 1994	Gergen et al.	395/375
☐	5371862	December 1994	Suzuki et al.	395/375

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY
57-114950	July 1982	JPX

OTHER PUBLICATIONS

DSP56000/DSP56001 Digital Signal processor User's Manual, pp. 7-20-7-21, Motorola.
DSP56116 Digital Signal Processor User's Manual, pp. 603, Motorola.
Ulrich Holtmann et al; "Experiments with Low-Level Speculative Computation Based on Multiple Branch Prediction;" IEEE Transaction on VLSI vol. 7, No. 3, Sep. 1993.

Tirumalai et al; "Parallelization of Loops with exist on Pipelined Architectures" Hewlett-Packard Laboratories; IEEE May 1990.

ART-UNIT: 232
PRIMARY-EXAMINER: An; Meng-Ai
ATTY-AGENT-FIRM: Lowe, Price, LeBlanc & Becker

ABSTRACT:

A pipeline processor having a hardware loop function, and having transfer paths L14 and L13 which directly transfer a value of a flag register 10 being set according to the results of the operations to a loop control unit 11, and so configured that the loop control unit 11 reads the value of the flag register 10 via the transfer paths L14 and L13 and terminates a loop processing when it is the predetermined value. The loop processing can be terminated without adversely affecting the data processing efficiency when a conditional jump instruction is executed during the loop processing, and operations, data transfers and other processings can be executed other than a loop-escaping operation.

4 Claims, 18 Drawing figures

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L22: Entry 18 of 18 File: USPT Mar 20, 1990

US-PAT-NO: 4910664
DOCUMENT-IDENTIFIER: US 4910664 A

TITLE: Data processor with apparatus for reducing loop processing time

DATE-ISSUED: March 20, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Arizono; Takeshi	Itami	N/A	N/A	JPX

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	N/A	N/A	N/A	JPX	03

APPL-NO: 7/ 126045
DATE FILED: November 27, 1987

INT-CL: [4] G06F 1/00
US-CL-ISSUED: 364/200; 364/260.4, 364/260.8, 364/262
US-CL-CURRENT: 712/241
FIELD-OF-SEARCH: 364/200, 364/900

REF-CITED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4429361	January 1984	Maccianti et al.	364/200
☐	4462074	July 1984	Linde	364/200
☐	4652997	March 1987	Kloker	364/200
☐	4792892	December 1988	Mary et al.	364/200

OTHER PUBLICATIONS

Intel Corporation (1983), "iPAX 286 Programmer's Reference Manual", pp. 3-21.fwdarw.-322.

ART-UNIT: 232
PRIMARY-EXAMINER: Zache; Raulfe B.
ATTY-AGENT-FIRM: Townsend and Townsend

ABSTRACT:

A data processing system with an apparatus for reducing loop processing time including an address reset circuit that resets the program counter and prefetch counter to the loop beginning address when the program executes the instruction at the loop ending address. The need for repeated address calculation for branching

the loop ending address. The need for repeated address calculation for branching to a loop beginning address after each loop execution cycle is eliminated, thereby speeding up the loop processing.

6 Claims, 10 Drawing figures

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"4792892".UREF..USPT.

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